Chips4Makers

Bootstrapping low-volume open source silicon
9/9/2017

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JOAT FibraServi bvba

Overview

- Chips want to be free
- The Dream
- Who Is So Crazy ?
- Pilot Project
- I need you!

Chips want to be free

- Linux: hackers (makers) coding at night on their PC

- For custom ASICs high start-up cost but now we have:

Crowdfunding

Distributed Development

KICKSTARTER

CROWD SUPPLY

GitHub

GitLab

The Dream

- Low-volume Open Source ASIC service

	Proprietary	Open Source
Commercial		ASICs
Non-profit Hobby		

More info in ‘RFC: is open source from Venus and commercial from Mars’ talk

The Dream

- Low-volume Open Source ASIC service
  - ASIC production targets high-volume: high startup costs, low per unit costs
    - Mask costs
    - EDA tools license
    - Engineering
    - IP blocks
    - The fine print is not maker friendly

The Dream

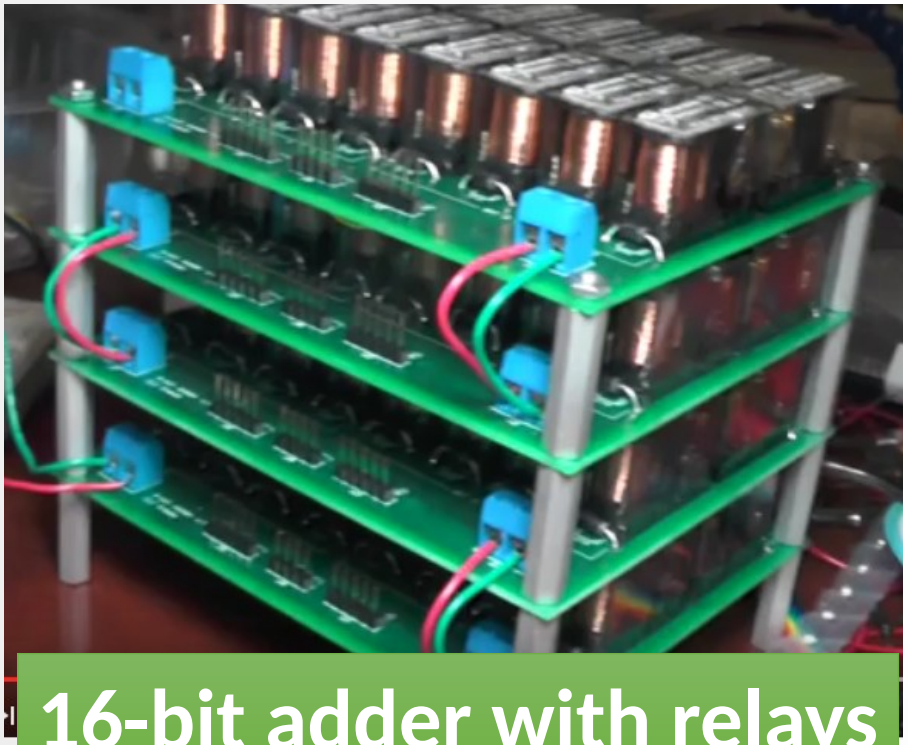
- Low-volume Open Source ASIC service
  - Cost < €100/piece for 100+ devices/boards; lower prices for higher volume
    - Open source RTL
      not reinvent/repay for the wheel
    - Pool different chips to share set-up cost; use multi-project wafer services
    - Push button open source EDA flow
    - Intermediate in the legal affairs

Who is so crazy ?

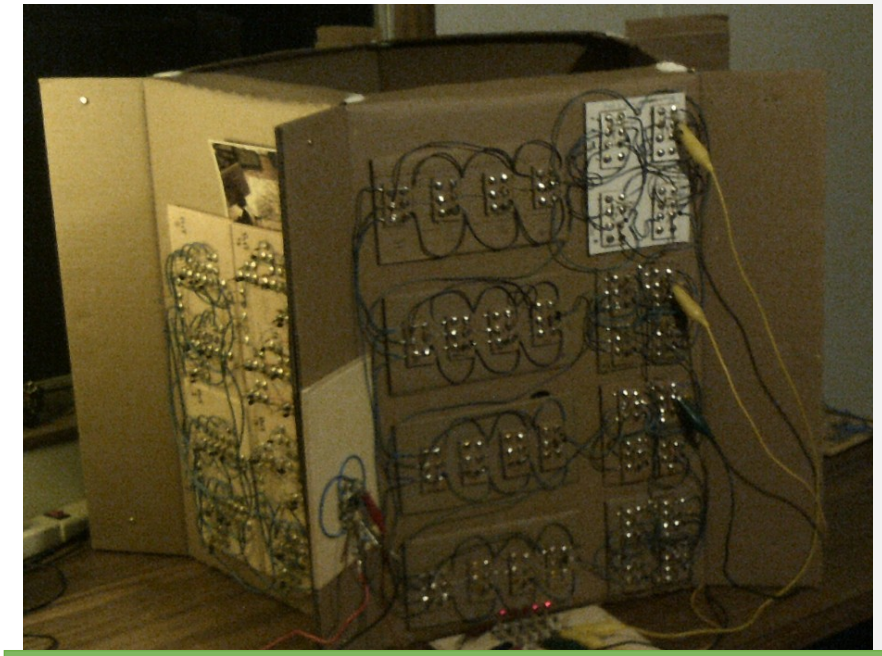
- Q: But can’t you do it with an FPGA ?

  A: Likely but not everyone wants to do it with a FPGA

Who is so crazy ?



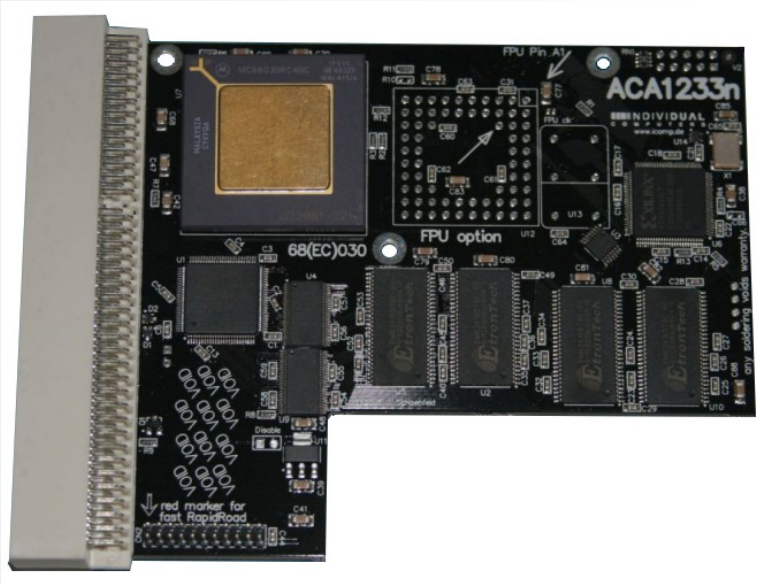
16-bit adder with relays



4-bit cardboard computer

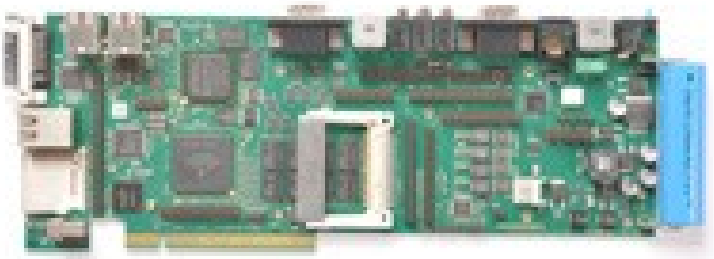
Who is so crazy ?

- Retro Computing



ACA 1233n 40Mhz Accelerator with 128MB RAM
€ 240,-

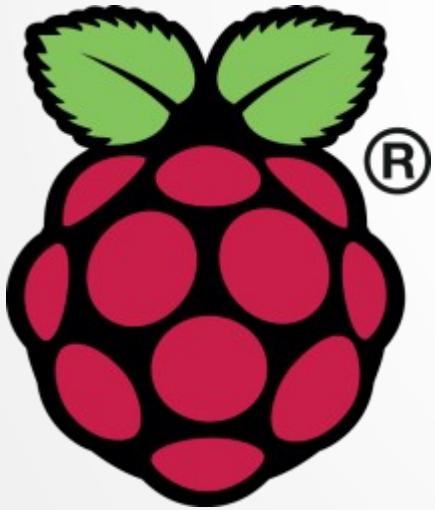
MIST FPGA computer simulates old consoles and computers
€ 200,-



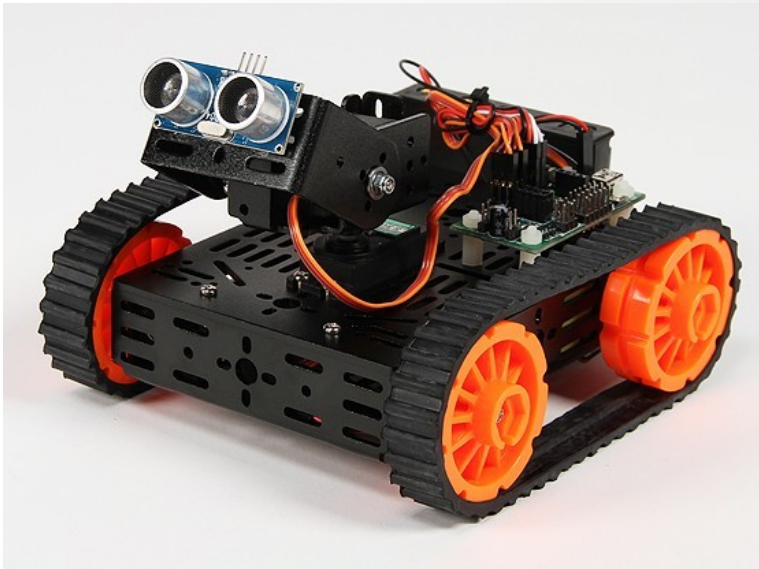
Firebee computer Coldfire based Atari clone
€ 520,-

Who is so crazy ?

- Hobbyist/Maker



Home Automation



Robotics

Pilot Project

- Why?
- What?
- Status
- Plans

Pilot Project

- Why ?
  - Find the shape of puzzle pieces
    - Start set of open source reusable RTL cores
    - Open source EDA flow
    - Startup cost reduction and sharing potential
    - Unmantling legal minefield
  - Stay independent from investors
    keep freedom to choose direction

Pilot project

- What ?

	Proprietary	Open Source
Commercial		Retro chips and boards
Non-profit Hobby		

Retro-uC

micro-controller with Z80, MOS6502, Motorola 68000 cores

Pilot Project

- Status
  - Selected cores T80 (Z80), T65 (MOS6502) and WF68K00IP (Motorola 68000)
    - Tested cores in FPGA retro computer and console projects (MIST, FPGA Arcade, SUSKA III, ...)
    - Permissive license to avoid complications of a copyleft license
    - VHDL
  - Demo
    - First top-level RTL on XLR8 with JTAG interface and Z80. Tested with buspirate.
    - https://gitlab.com/chips4makers/retro-uc

*imec also happens to be my day job employer

Pilot Project

- Status
  - Incorporated own company FibraServi bvba
    - Needed to handle the fine print
  - Under discussion with imec* on process options
    - Determine layout chips/boards and the crowdfunding pledge levels
    - Determine stretch goals
  - Crowdsupply pre-launch page: https://www.crowdsupply.com/chips4makers/retro-uc
    - Target for start goal below € 50000

*imec also happens to be my day job employer

Pilot Project

- Plans
  - Nov. 2017: launch crowdfunding campaign
  - Jan. 2018: end of campaign;
    start implementation for reached stretch goal
  - Q2 2018: tape-out chip
  - ORConf 2018: present (first) boards

I need you!

- Support the crowdfunding campaign
- Help with implementation, EDA software, …
- Pointers:
  - staf@fibraservi.eu
  - https://gitlab.com/chips4makers/retro-uc
  - https://www.crowdsupply.com/chips4makers/retro-uc
- But…
  I can’t clone myself and don’t multitask well